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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,559	06/29/2001	Jong Sang Back	8733.448.00	5057
30827 7590 05/13/2008 MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			EXAMINER BECK, ALEXANDER S	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 05/13/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

09/893,559

**Applicant(s)**

BAEK ET AL.

**Examiner**

Alexander S. Beck

**Art Unit**

2629

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 12-35 is/are pending in the application.
- 4a) Of the above claim(s) 18-35 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 12-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/C)
- Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

1. Acknowledgment is made of the amendment filed Jan. 28, 2008 ("Amend."), in which claims 12, 14 and 16 are amended and the rejections of the claims are traversed. Claims 12-35 are currently pending, of which claims 18-35 are withdrawn, and an Office action on the merits follows.

### ***Claim Rejections - 35 USC § 103***

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
4. Claims 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,279,035 to Skerlos ("Skerlos") in view of U.S. Patent No. 5,686,846 to Holcomb et al. ("Holcomb") and U.S. Patent No. 5,713,040 to Lee ("Lee").

As to claims 12, 14 and 16, Skerlos discloses a method of driving a display comprising: receiving an input signal having a first period corresponding to a number of

lines in the display; and comparing the first period with a reference period (Skerlos, col. 11, ll. 12-18). Moreover, Skerlos discloses outputting a signal of a first state (e.g., 'ok pulse flag') only if the first period is indicative of an input signal presence (e.g., vsync); and determining the absence or the presence of the input signal according to the number of the signal of the first state during a predetermined interval (e.g., number of pulses, at least one for presence and none for absence) (Skerlos, Table 1). As to the method of determining the absence or the presence, Skerlos does not disclose expressly if the number of continuous pulses of the signal of the first state is *not less than a predetermined plural number*. Rather, Skerlos merely discloses determining the absence or the presence if the number of the signal of the first state (e.g., pulse number) is *not less than one*. However, Holcomb discloses a method of detecting the presence of a single pulse with edge detect circuits that generate pulses in response to both rising and falling edges of a signal (e.g., a rising and falling edge constitute a single pulse) (Holcomb, col. 4, ll. 12-14.)

All of the claimed teachings are known in Skerlos and Holcomb. The only difference is the combination of the "old teachings" into a single method of determining the absence or presence of a vertical synchronization signal in a display device. Thus, it would have been obvious to one having ordinary skill in the art to provide the edge detect circuit taught by Holcomb into the teachings of Skerlos for the purpose of detecting the presence (or absence) of an 'ok pulse flag' based on the number of detected rising/falling edges (e.g., two total rising/falling edges for a single pulse), and generating a pulse in response to each rising and falling edge. This would have been obvious because the operation of an edge detect circuit is in no way dependent on the operation of the other circuitry in Holcomb, and an edge detect circuit could be used in combination with any received signal to achieve the predictable results of determining the presence (or absence) of a pulse.

As such, Skerlos as modified by Holcomb teaches/suggests determining the absence or the presence of the input signal (e.g., vsync signal) if the number of *continuous pulses of* the signal (e.g., an 'ok pulse flag' will have two continuous pulses, a first pulse for the detection of a rising edge and a second pulse for a falling edge) of the first state is not less than a predetermined plural number (e.g., 2) during a predetermined interval. For example, examiner respectfully submits that when a vsync signal is detected then an 'ok pulse flag' is generated (Skerlos, Table 1), and when an 'ok pulse flag' is detected by an edge detect circuit then two continuous pulses – a first pulse for a detected rising edge and a second pulse for a detected falling edge – are generated (Holcomb, col. 4, ll. 12-14.; see also col. 5, ll. 36-39). Two continuous pulses are indicative of vsync signal presence, whereas anything less than two continuous pulses are indicative of vsync signal absence. Thus, a presence of a vsync signal is determined if the number of continuous pulses of the signal output by the edge detect circuit is not less than 2.

Moreover, Skerlos does not disclose expressly wherein the comparing of the first period with a reference period includes: determining only whether the first period is less than a first reference period; determining only whether the first period is greater than a first reference period; or determining only whether the first period is less than a first reference period and greater than a second reference period. Lee discloses a method of detecting the absence or the presence of different v-sync signals in Figures 3A and 3B, comprising: receiving an input signal having a first period corresponding to a number of lines in the display; determining only whether the first period is less than a first reference period; determining only whether the first period is greater than a first reference period; and determining only whether the first period is less than a first reference period and greater than a second reference period (Lee, col. 4, ll. 7-67).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the teachings of Skerlos and Holcomb such that the comparing of the first period with a reference period includes: determining only

whether the first period is less than a first reference period; determining only whether the first period is greater than a first reference period; and determining only whether the first period is less than a first reference period and greater than a second reference period, as taught/suggested by Lee. The suggestion/motivation for doing so would have been to detect the absence or the presence of a v-sync signal in the event that v-sync signals of more than one value may be received by the display (Lee, col. 1, l. 58 – col. 2, l. 12).

As to claims 13, 15 and 17, Skerlos discloses wherein the receiving, determining and outputting steps are repeated and determining if the first state is output a second time (Skerlos, col. 13, ll. 7-12).

### ***Response to Arguments***

5. Applicant's arguments filed Jan. 28, 2008, have been fully considered but they are not persuasive. Applicant argues that the edge detect circuit 19a and 19b of Holcomb generate the pulses for only one pulse because the edge detect circuit 19a detects the falling edge of the signal A and outputs signal E1 whereas the edge detect circuit 19b detects the rising edge of the signal B and outputs signal E2 (Amend., p. 7). However, examiner respectfully submits that the edge detect circuit 19a of Holcomb may be, for example, output signal E1 which comprises pulses generated for both each rising and falling edge of a signal (Holcomb, col. 5, ll. 36-39). Thus, two continuous pulses are output by the edge detect circuit of Holcomb in response to a detected rising and falling edge of a signal.

Furthermore, as noted in the rejection of claims 12, 14 and 16 above, examiner respectfully submits that Skerlos and Holcomb taken collectively would fairly suggest to one of ordinary skill in the art, determining the absence or the presence of an input signal (e.g., vsync signal) if the number of *continuous pulses* of the signal (e.g., an 'ok pulse flag' will have two continuous pulses, a first pulse for the detection of a rising edge and a

second pulse for a falling edge) of the first state is not less than a predetermined plural number (e.g., 2) during a predetermined interval. A more detailed explanation can be found in the rejection of claims 12, 14 and 16 above.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander S. Beck whose telephone number is (571)272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/  
Supervisory Patent Examiner, Art Unit 2629

asb  
May 8, 2008